W&B Ref. No.: INF 2071-US Atty. Dkt. No. INFN/WB0040

IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously Presented) A method for producing an antifuse structure in a substrate, comprising:

forming a conductive region in the substrate, the conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge;

forming a nonconductive region adjoining the conductive region in the substrate, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface; and

forming a dielectric layer over at least a portion of the first upper surface of the conductive region, at least a portion of the edge, and at least a portion of the second upper surface, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer.

- 2. (Original) The method of claim 1, forming a conductor on the dielectric layer.
- 3. (Original) The method of claim 1, wherein the conductive region defines a corner and wherein forming the dielectric layer comprises forming the dielectric layer over the corner.
- 4. (Original) The method of claim 1, wherein the first lateral boundary surface is substantially orthogonal to a lower surface of the dielectric layer interfacing with the edge.
- 5. (Original) The method of claim 1, wherein the conductive region is a doped semiconductor region.

- 6. (Original) The method of claim 1, wherein the nonconductive region comprises at least one of SiO₂ and SiN.
- 7. (Original) The method of claim 1, wherein the dielectric layer comprises SiN.
- 8. (Original) The method of claim 1, wherein the nonconductive region comprises at least one of SiO₂ and SiN and wherein the dielectric layer comprises SiN.
- 9. (Original) The method of claim 1, wherein the dielectric layer is disposed over at least a portion of the nonconductive region.
- 10. (Currently Amended) A method of blowing an antifuse, comprising:
 - a) providing an antifuse, comprising:
 - a conductive region <u>formed in a substrate</u>, the conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge;
 - a nonconductive region adjoining the conductive region, the nonconductive region, formed in a substrate, defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface; and
 - a dielectric layer disposed over at least a portion of the first upper surface of the conductive region, at least a portion of the edge, and at least a portion of the second upper surface; and
- b) applying a programming voltage to the antifuse to form a breakdown channel in the dielectric layer, whereby an area of relatively increased field strength is produced along the edge.
- 11. (Original) The method of claim 10, wherein the conductive region defines a corner and wherein the dielectric layer is disposed over the corner and wherein applying the programming voltage results in a further area of relatively increased field strength.

- 12. (Original) The method of claim 10, wherein the dielectric layer is disposed over at least a portion of the nonconductive region.
- 13. (Original) The method of claim 10, wherein the antifuse further comprises a conductor on the dielectric layer.
- 14. (Currently Amended) An antifuse, comprising:

a first conductive region, the first conductive region defining a first upper surface and a first lateral boundary surface which meet at an angle to form an edge;

a nonconductive region adjoining the first conductive region, the nonconductive region defining a second upper surface and a second lateral boundary surface; wherein the first and second lateral boundary surfaces are in facing relationship and form an interface:

a dielectric layer disposed over at least a portion of the first upper surface of the first conductive region, at least a portion of the edge, and at least a portion [[fo]] of the second upper surface, whereby an area of relatively increased field strength is produced during application of a programming voltage to form a breakdown channel in the dielectric layer; and

a second conductive region on the dielectric layer.

- 15. (Original) The antifuse of claim 14, wherein the first conductive region defines a corner and wherein the dielectric layer is disposed over the corner.
- 16. (Original) The antifuse of claim 14, wherein the first conductive region and the nonconductive region form a substantially planar upper surface which interfaces with a lower surface of the dielectric layer.
- 17. (Original) The antifuse of claim 14, wherein the dielectric layer is disposed over at least a portion of the nonconductive region.

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18. (Original) The antifuse of claim 14, wherein the nonconductive region comprises at least one of SiO₂ and SiN.

- 19. (Original) The antifuse of claim 14, wherein the dielectric layer comprises SiN.
- 20. (Original) The antifuse of claim 14, wherein the nonconductive region comprises at least one of SiO₂ and SiN and wherein the dielectric layer comprises SiN.
- 21. (Previously Presented) A method for producing an antifuse structure in a substrate, comprising:

forming a first conductive region in the substrate, the conductive region defining a first upper surface and lateral boundary surfaces that meet and form a corner;

forming a nonconductive region in the substrate adjoining the conductive region, the nonconductive region defining a second upper surface and lateral boundary surfaces that meet at the corner of the conductive region;

forming a dielectric layer on the first and second upper surfaces overlapping at least the corner of the conductive region; and

forming a second conductive region on the dielectric layer overlapping the corner of the conductive region, whereby an area of relatively increased field strength is produced during application of a programming voltage to first and second conductive regions to form a breakdown channel in the dielectric layer proximate the corner.

- 22. (Previously Presented) The method of claim 21, wherein the first lateral boundary surface is substantially orthogonal to a lower surface of the dielectric layer interfacing with the edge.
- 23. (Previously Presented) The method of claim 21, wherein the conductive region is a doped semiconductor region.

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24. (Previously Presented) The method of claim 21, wherein the nonconductive region comprises at least one of SiO₂ and SiN.

- 25. (Previously Presented) The method of claim 21, wherein the dielectric layer comprises SiN.
- 26. (Previously Presented) The method of claim 21, wherein the nonconductive region comprises at least one of SiO₂ and SiN and wherein the dielectric layer comprises SiN.